INNOVATIVE ARCHITECTURES FOR DENSE MULTI-MICROPROCESSOR COMPUTERS

Dr. Robert E. Larson
Chairman and C. E. O.
Expert-EASE Systems, Inc.
Belmont, California 94002

The purpose ~~of this presentation~~ is to summarize a Phase I SBIR project performed for the ~~NASA~~/Langley Computational Structural Mechanics Group. The project was performed from February to August 1987.

The main objectives of the project were to:

1. Expand upon previous research into the application of "chordal ring" architectures to the general problem of designing multi-microcomputer architectures.
2. Attempt to identify a family of chordal rings such that each chordal ring can be simply expanded to produce the next member of the family.
3. Perform a preliminary, high-level design of an expandable multi-microprocessor computer based upon chordal rings.
4. Analyze the potential use of chordal ring based multi-microprocessors for sparse matrix problems and other applications arising in computational structural mechanics.

PRESENTATION OVERVIEW

- Corporate Capabilities
- Transputer Hardware
- Interconnection Architecture
- Applications
- User Interface

PRESENTATION OVERVIEW

This presentation covers the following topics:

1. The Corporate Capabilities of Expert Ease Systems. Particular emphasis will be placed on the company's driving objective to use projects such as this one as stepping stones to develop products which can compete and thrive in the American and International marketplaces.

2. Transputer Hardware Specifications. The T800 Transputer microprocessor recently introduced by Inmos Corporation is a very powerful chip that is ideally suited for multi-microprocessor architectures. Inmos has published their Transputer specifications widely, and a substantial amount of information can be obtained directly from the company.

3. Interconnection Architecture. The critical goal of this Phase I SBIR project was to investigate novel interconnection architectures called "chordal rings". Chordal rings have several very interesting properties that make them particularly competitive with other architectures commonly cited as potential multi-microprocessor architectures, especially the hypercube upon which Intel has based its PSC. In particular, chordal ring "families" have been identified. Each chordal ring in the family can be easily expanded into the next larger ring in the family.

4. Applications of a Choral Ring-Based Multi-Microprocessor. The talk presents a summary of several interesting examples of how a chordal ring computer could be used to solve problems of interest in computational structural mechanics.

5. User Interface. Expert-EASE Systems has several software products which incorporate powerful, user-friendly interfaces. Such interfaces are emphasized in our projects for both corporate and government clients. Indeed, the development of this type of interface has been emphasized in our Phase II proposal to develop a chordal ring-based multi-microprocessor which can be expanded from 10 to over 1000 T800 Transputer chips.

In summary, then, I will summarize the substantial progress made during Phase I, especially how we have demonstrated the feasibility and advantages of a multi-microprocessor machine based upon chordal ring architecture.

CORPORATE OVERVIEW

Expert-EASE Systems

- o Product-Oriented Company
- o Expertise
  - Distributed Computing
  - Software Design
  - User Interfaces
  - Artificial Intelligence
- o Previous Phase II Successes
  - Pantheon
  - EASE+NEXPERT

Phase II Project Managers

- o Dr. Robert E. Larson, Principal Investigator
  - 1982 IEEE President
  - Founder/President of Systems Control, Inc., Palo Alto, California
  - Stanford Professor
- o Dr. John G. O'Reilly, Assistant Principal Investigator
  - DMS for Space Station
  - Extensive Networking and Real-Time Computing Experience
- o Dr. Sidney Fernbach, Applications Consultant
  - Former Head, Physics and Computing, LLL
  - Supercomputer Expert (DOD, DOE, NSF)

CORPORATE OVERVIEW

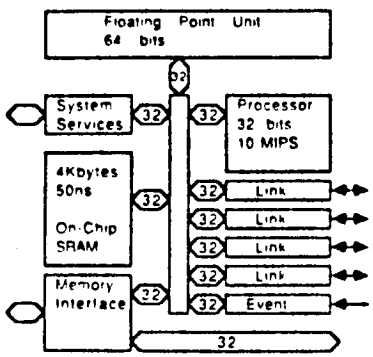
Expert-EASE Systems is a product-oriented company with strong personnel and a proven track record in several areas of particular interest to researchers in computational structural mechanics. These areas include: distributed computing, especially the design of distributed architectures and distributed data bases; software design for all types of computers, from microcomputers to Crays; user interface design, including natural language interfaces; and artificial intelligence, particularly knowledge-based expert systems.

Expert-EASE Systems has a proven track record of developing and marketing commercially available software products. We now have twenty products in our "EASE+" family of microcomputer based programs. These have proven very successful in several industries, including electric utilities, process control, defense and aerospace, manufacturing, and artificial intelligence.

Further, we have developed two commercially successful products as a direct consequence of the SBIR program. First, we developed a natural language program to simultaneously access multiple data bases residing on multiple heterogeneous computers. This product, called Pantheon, led directly to the formation of a subsidiary company, Pantheon Systems. Second, a DOE Phase II award led to the integration of our EASE+ interface with a widely used expert system, NEXPERT, produced by Neuron Data, Inc. We estimate that this product, which we call EASE+NEXPERT, will have first year sales in excess of $1,000,000.

Now that I have presented an introduction to our general capabilities, I'd like to present our specific qualifications to perform our proposed Phase II effort. The effort will involve three managers, each of whom has years of experience developing computers based upon novel architectures. The managers include: myself, I have spent over 25 years working on both distributed and centralized approaches to solving computationally intensive problems in many different fields; Dr. John G. O'Reilly, a distributed computer expert with whom I've worked for nearly 10 years and have had the opportunity to coauthor two books on distributed computing; and Dr. Sidney Fernbach who is generally considered one of the world's leading experts on supercomputers.

IMS T800 FLOATING POINT TRANSPUTER



- 32 - bit processor
- 15 MIPS
- 64-bit on-chip floating point processor
- 4K on-chip high speed RAM
- Four 20Mbits/sec communication links. (On-chip)
- Sustained 2.25 MFLOPS (30 Mhz).
- On-chip memory controller

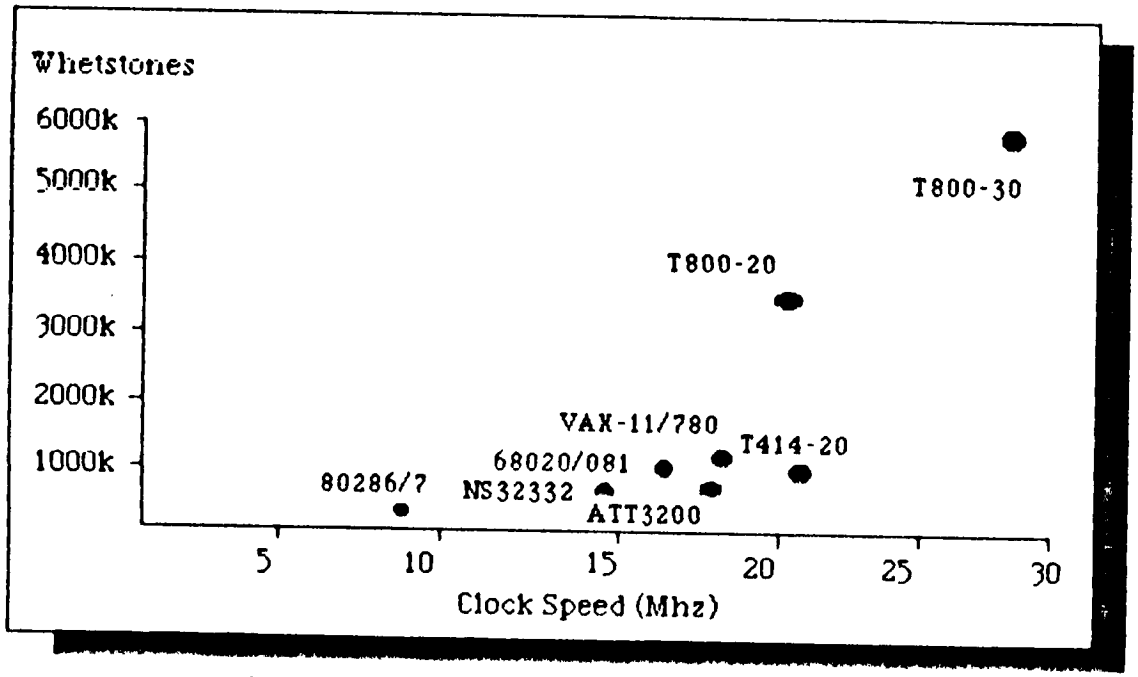
IMS T800 FLOATING POINT TRANSPUTER

After extensive evaluations of a number of leading multiprocessor chips, the Inmos T800 transputer was selected as the basis of the choral ring-based multi-microcomputer to be built during Phase II.

The T800 combines high computational performance, adequate on-board memory, excellent communications facilities, and low cost. Some of the outstanding features of the transputer include:

- A high processing rate (10 MIPS/1.5 MFLOPS for the 20MHz chip and 15 MIPS/2.25 MFLOPS for the 30MHz version)
- An on-chip 64-bit floating point processor
- Four 20 Mbits/sec on-chip communication links

T800 FLOATING POINT PERFORMANCE



T800 FLOATING POINT PERFORMANCE

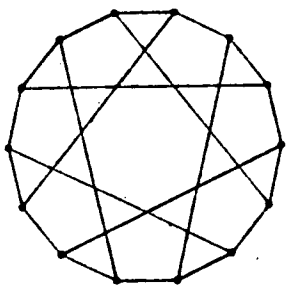
The computational power of the Transputer compares with that of other well-known microprocessors in this figure. The measure of computational power is taken to be Whetstones per second, which considers the execution of a mixture of operations that is representative of what might be encountered in an actual program. This measure is preferable to millions of instructions per second (MIPS) or millions of floating point operations per second (MFLOPS); however, the Transputer has similar advantage in terms of these measures.

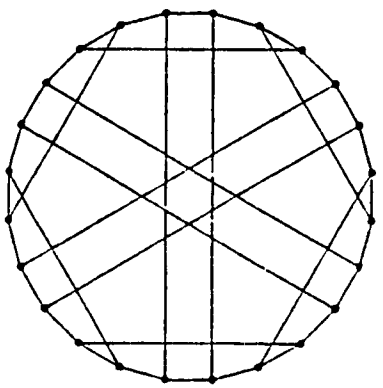
As can be seen from the figure, the 30 MHz T800 (denoted as T800-30) and the 20 MHz T800 (denoted as T800-20) are both far more powerful than the leading microprocessors made by Intel (80286/87), Motorola (68020/081), National Semiconductor (NS32332) and AT&T (ATT 3200). Note that those microprocessors are also far more powerful than the Digital Equipment Corporation VAX 11/780, a well-known minicomputer. Finally, the T800-20 and T800-30 are substantially superior to the previous generation Transputer, the T414-20.

PROPERTIES OF
CHORDAL RINGS

n = Nodes - Number of microprocessors in network
k = Diameter - Maximum distance between any two nodes.
d = Degree - Number of communication channels on each node.

- Shorter network diameter with larger number of nodes.
- Even distribution of network traffic.
- Efficient use of resources.





PROPERTIES OF THE CHORDAL RINGS

The investigation of multi-microprocessor architectures is typically performed as a graph theoretic problem in which the objective is to find a way in which n nodes can be interconnected so as to maximize some quantitative function of the architecture. In this formulation, each node represents a single processor and each link represents a communications channel connecting two processors.

Three terms from graph theory are commonly used to describe computer architectures:

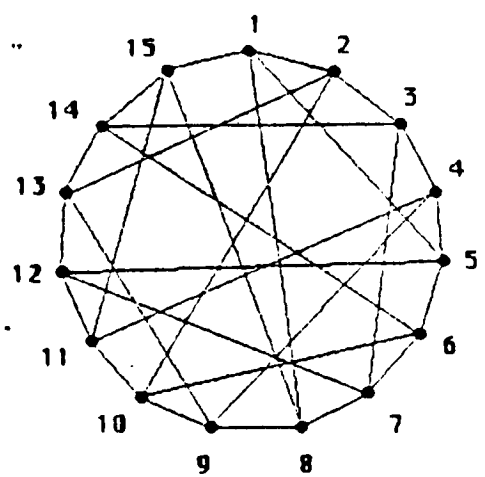
- The number of microprocessors in a given architecture is denoted by n. Although the individual microprocessors need not be identical, we, along with virtually all other researchers in the field, consider only architectures in which the nodes are identical.
- The diameter, k, of a graph is the number of links separating the two nodes which are furthest apart in the graph.
- The degree, d, of a graph is the number of nodes to which each node is connected. Again, in our research, we have assumed that all nodes in the graph are connected to the same number of other nodes in the graph.

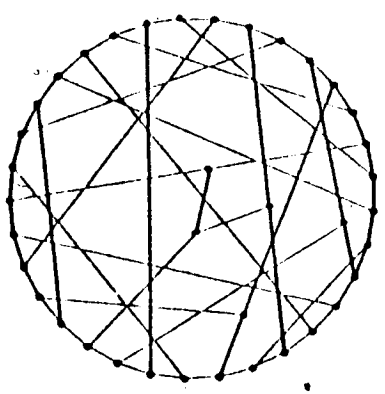
Chordal rings have several properties which are of high value from the perspective of a multi-microprocessor architecture. Specifically, chordal rings:

- Provide large n for fixed values of d and k
- Allow for the even distribution of network traffic
- Provide for the well-balanced, efficient use of network resources, including node throughput and link bandwidth

MODIFIED CHORDAL RING

- Maintains significant characteristics of Chordal Ring
- Easily expandable with minimal reconfiguration
- Uniform growth path (10,15,36,78...).





MODIFIED CHORDAL RING

Our research was not limited to pure chordal rings, which, by definition possess rotational symmetry. Instead, we emphasized the analysis of "modified chordal rings" which: (a) (left figure) may or may not possess rotational symmetry, and (b) may not even be rings (right figure).

It is by breaking away from the constraints imposed by pure chordal rings that we were able to derive graphs with particularly good architectural attributes. Indeed, it was found that:

- Modified chordal rings provide virtually all of the good attributes of pure chordal rings, while providing substantially higher values of n for fixed values of d and k.
- Modified chordal rings can be assembled into families in which a given graph can be expanded to the next larger graph in the family by the addition of nodes and links in a reasonably well-defined manner.
- The growth path for these modified chordal rings can be selected to have a high level of uniformity. From a commercial marketing aspect, this permits computers to be designed so that they can be continually expanded by the user in appropriate increments when his needs require.

COMPARISON OF CHORDAL RINGS AND HYPERCUBES

- REDUCED DATA COMMUNICATIONS -

		Hypercube		Chordal Ring	
n	d	k	<p>	k	<p>
150 8	3	3	1.5	2	1.375
16	4	4	2.0	3	1.719
32	5	5	2.5	3	2.016
64	6	6	3.0	3	2.328
128	7	7	3.5	4	2.580
256	8	8	4.0	4	2.776

PARAMETERS CONSIDERED

COMPARISON OF CHORDAL RINGS AND HYPERCUBES

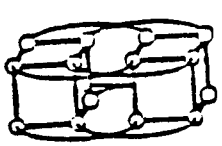
This chart is fairly self-explanatory. However, the main conclusion which should be drawn is:

- For fixed n and d, the chordal ring has significantly lower values of k and d (mean distance between nodes) than the corresponding hypercube.

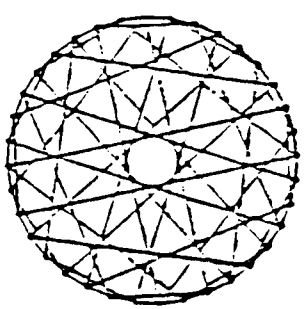
COMPARISON OF CHORDAL RINGS AND HYPERCUBES

- INCREASED PROCESSING POWER (2.25 X) -

Level	Hypercube		New Chordal Ring Family	
	Nodes	Diameter	Nodes	Diameter
1	8	3	10	2
2	16	4	15	2
3	32	5	36	3
4	64	6	78	4
5	128	7	166	5
6	256	8	348	6
7	512	9	742	7



d=4, k=4 HYPERCUBE



d=4, k=3 CHORDAL RING

COMPARISON OF CHORDAL RINGS AND HYPERCUBES

This chart compares the new family of chordal rings with the standard hypercube graphs. It is clearly evident that for approximately equal computing power (i.e., numbers of nodes) the chordal rings possess substantially reduced diameter, and hence, would have fewer messages relayed between nodes.

The chart could also be interpreted with respect to a fixed diameter. That is, given a hypercube and a chordal ring with the same diameter, the chordal ring possesses substantially increased computing power via its many more nodes.

APPLICATIONS

- Primary Application: Computational Structural Mechanics
  - Finite Element Analysis (2-D and 3-D)
  - Problems of Importance to NASA
- Mathematical Operations:
  - Sparse Matrix Operations
    - Banded
    - Irregular
  - Eigenvalue Operations
- Secondary Applications:
  - Control Systems Analysis
  - Stability Analysis
  - Optimization/Mathematical Programming
  - Signal Processing
  - Image Processing

APPLICATIONS

Shown on this slide are only a few of the many computationally intensive problems which may be solved on multi-microprocessors. We believe that our chordal ring approach provides substantially reduced computing time compared to other architectures due to its superiority in communications and throughput for given n, d, and k.

USER INTERFACE

Requirements:

- Transportability. System must be able to run current NASA software with minimal or no modification.

- Efficiency. Computing tasks with high parallel content are performed as function calls to transputer network, while sequential tasks can run on front-end processor.

- Ease-of-Use. Tools should be provided to facilitate use of system by non-specialists.

USER INTERFACE

Our Phase II proposal outlined the development of a multi-microprocessor computer based upon a family of expandable chordal ring architectures. However, as I've tried to stress throughout this presentation, Expert-EASE Systems places a strong emphasis on the "usabililty" of the systems it develops. We were founded as a company in order to design, develop, and market an excellent IBM-PC based user interface to large, unwieldy codes residing on mini-computers and mainframes. Although, over the past few years our corporate direction has broadened and our technical capabilities have grown, we continue to emphasize highly user-friendly interfaces.

With this in mind, we have identified three central criteria which define the extent of the user interface required by our chordal ring based multi-microprocessor, if it is to be successfully incorporated into the computational environment at NASA/Langley, NASA/Lewis, as well as other similar establishments throughout the U.S.

These requirements are:

- Transportability. The system must be able to run all current NASA software with minimal or no modification. This requirement is derived from the NASA/Langley CSM group's desire to devote their efforts to research and not have to interrupt the flow of that work in order to utilize another computer.

- Efficiency. The chordal ring computer will operate in a "back-end" configuration with a VAX. In this configuration, specific computing tasks with high parallel content will be performed as a function calls to the back-end computer. For example, the function calls will include matrix invertion, addition, multiplication, etc. Computing tasks which are largely sequential in nature will execute on the front end VAX.

- Ease-of-Use. Tools (e.g., a large library of function calls) will be provided to facilitate the use of the system by researchers who are not parallel programming experts.

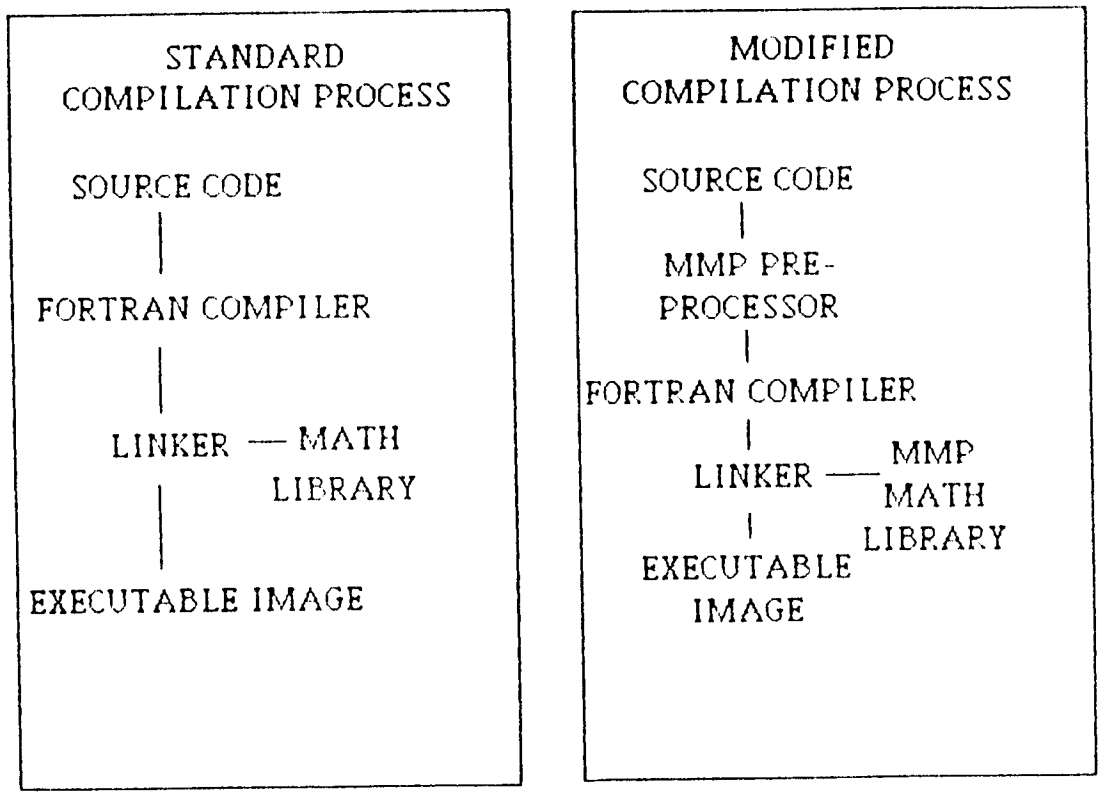
PROPOSED SOLUTIONS

- MicroVAX platform
- MMP Pre-processor
- MMP math library
  - EES routines
  - Routines developed by NASA and the user community.
- EASE+
  Graphics oriented front-end for input.
  Graphics oriented post processor for display and data visualization.
- CAD interface

PROPOSED SOLUTIONS

Based upon the high-level requirements just presented, a design approach which results in a very effective back-end, chordal ring-based multi-microprocessor has been developed. Shown on the slide is a brief list of features which will be incorporated into the computer system. These specifications have been derived to: (1) minimize the time and effort required to integrate the computer into the existing research environment at NASA/Langley, and (2) maximize the effectiveness of the system once it is installed.

MMP PREPROCESSOR MAKES MODIFICATIONS TRANSPARENT TO THE PROGRAMMER



MMP PRE-PROCESSOR

This slide indicates the method by which software will be compiled for execution on the new chordal ring-based computer. It is constrasted to the standard compilation processes. The major differences between the two methods are:

- A pre-processor will convert specific multi-microprocessor calls (e.g., matrix inversion) to a form that can be handled by the FORTRAN compiler. The pre-processor will be designed so that its use requires minimal effort on the part of the researchers.

- A library of mathematical function calls will be developed. Time and cost constraints during Phase II clearly limit the number of functions that can be developed. However, we will work closely with NASA/Langley CSM Group to identify the functions of maximum utility to them. Over time, the library can be expanded by the CSM Group, Expert-EASE Systems, and other users of the system.

DESCRIPTION OF EASE+

- o Intuitive user interaction
- o Graphics Database
  - Icons/Objects linked to database
  - Dynamic colors driven by any data
  - Built-in sophisticated plotting
- o Full Featured Database, Menus & Forms
- o Powerful Procedural Language
- o Tools that Support Rapid Development

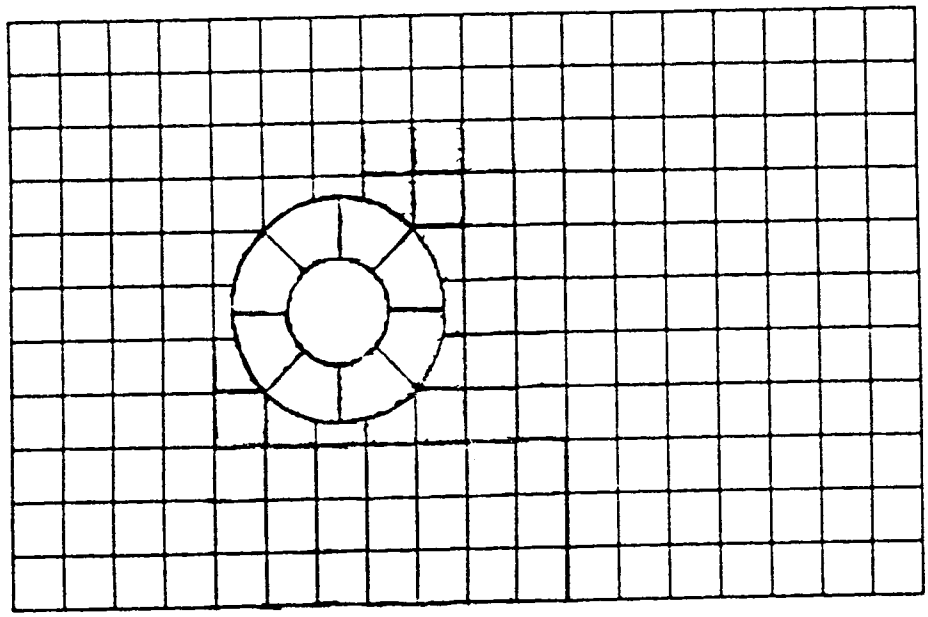
DESCRIPTION OF EASE+

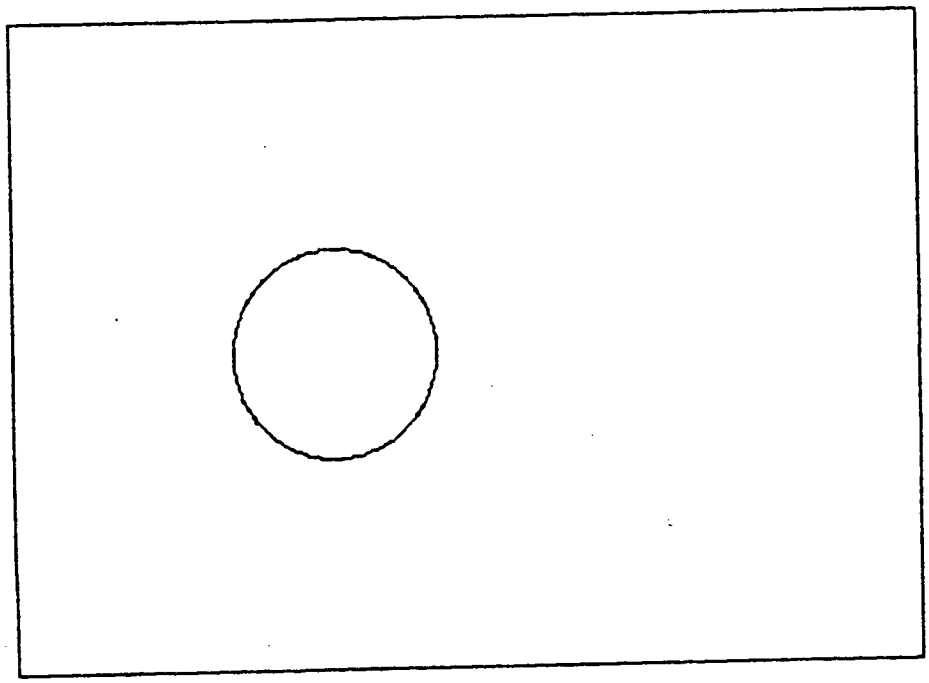
During this talk I've alluded to the general features of the EASE+ *nterface my company has produced. This slide highlights several of the main EASE+ features.

Essentially, EASE+ is a powerful set of software tools that permit users to define highly interactive graphics displays. Users can define icons to represent a desired object; the icons can then be linked to each other or to a database. In this manner, interactions representing highly complex physical processes can be displayed precisely and accurately.

EASE+ emphasizes the use of inter-related menus, forms, and windows. Users are, for example, permitted to open multiple windows containing data on a specific icon or set of icons. Finally, EASE+ permits the rapid definition of many types of graphs, figures, plots, and charts.

In summary, EASE+ is a powerful set of software tools with which users can define and develop accurate, high resolution, highly inter-active displays of processes and data. The utility of EASE+ has been proven in the market place; sales for 1988 will be in excess of $2,000,000.



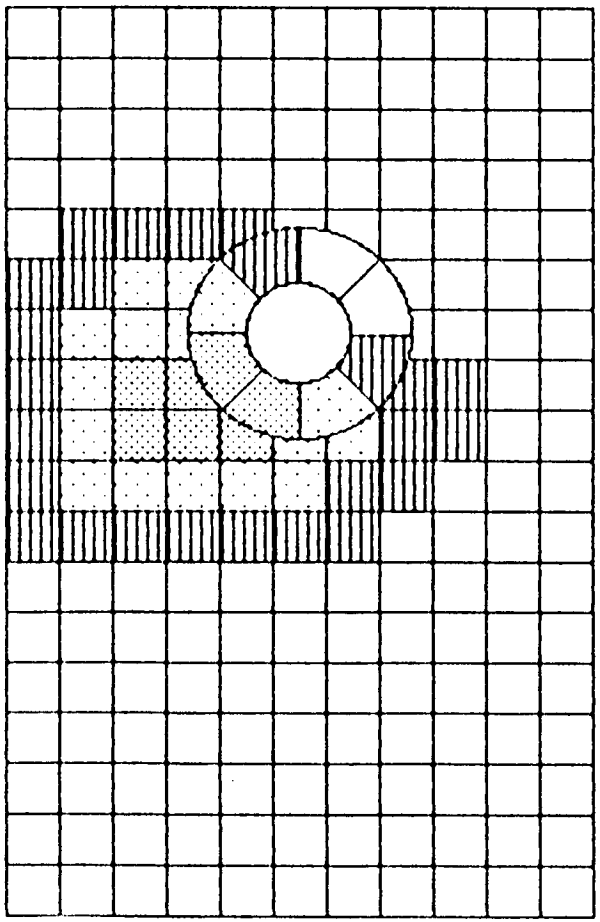


EASE+ PRE-PROCESSING

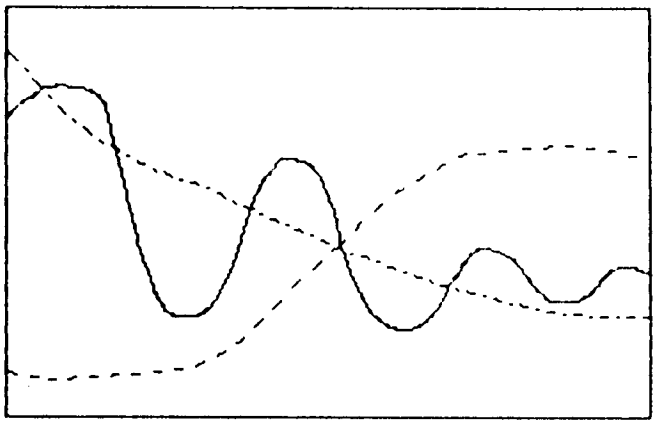
Shown on the left part of this slide is a representation of the blade panel which is of high interest to the CSM Group. For simplicity, no stiffeners have been included in the diagram.

On the right part of the slide is a very coarse grid model of the panel. The local grid around the hole is representative of the meshes being used in the plate research currently being performed.

EASE+ POST-PROCESSING



Shaded Squares are
Regions of Critical Stress



xa = ———
xb = - - - - - -
xc = -·-·-·-·-

Plots of Time
Variation Functions

EASE+ POST-PROCESSING

Represented on the left part of this slide is the result of a stress analysis for the blade panel. For the sake of this example, only four different types of stress regions have been identified. In the chordal ring multi-microprocessor with an EASE+ user interface, this plot would be shown on a high resolution (e.g., 1280 x 1024) color CRT. Many different stress regions could be indicated by user-defined colors.

The value of EASE+ is that it would allow the user to analyze and display the stress results from different stress regions via a mouse. The user could select a particular stress region and a graph of time variations of selected functions (e.g., xa, xb, xc) in that region would be displayed in high resolution color graphics. Further, functions from different stress regions could be displayed in the same plot. Results may also be plotted via bar-graphs, charts, or other representations defined by the user.

EASE+ does not provide anything that can not be developed by an individual user using standard FORTRAN, "C" or other programming languages. However, the advantage of using EASE+ as the user interface is that it permits a higher level of system functionality to be implemented during Phase II than would otherwise be feasible. Indeed, EASE+ is the result of dozens of man-years of development time. It has evolved as the result of continual feedback from hundreds of end-users.

In summary, incorporation of EASE+ into the Phase II chordal ring multi-microprocessor would allow the computer to have an immediate impact upon the research activities of groups at both NASA/Langley and NASA/Lewis.

SUMMARY

1. Innovative Multi-Microprocessor Computer Design Based on:

   - Inmos Transputer Chip
     - Powerful (T800 version)
     - Well-Supported

   - Modified Chordal Ring Architecture
     - Expandable
     - Low Internodal Distances
     - Low Connection Degree

   - Packaging Concept
     - Low Cost Base System (10 processors)
     - Incrementally Expandable to Over 1000 processors

2. Effective Software

   - Transportability of Existing Code
     - MICROVAX Platform
     - MMP Pre-Processor

   - Efficient Utilization of MMP
     - MMP Library
     - Function Calls

   - User-Friendly Interface
     - EASE+
     - CAD Interface
     - Visual Programming Input

SUMMARY

During this presentation I've attempted to summarize the proposed Phase II effort to develop a chordal ring multi-microprocessor system.

The system's hardware is based upon

- The very powerful Inmos T800 Transputer
- A modified chordal ring architecture interconnection structure that has low internodal distances and low connection degree
- A powerful packaging concept that provides a small, low cost base system of 10 Transputers, but can be expanded in a step-wise manner to over 1000 processors

The Phase II effort will emphasize the development of

- A software preprocessor to permit the utilization at existing CSM code
- A library of powerful function calls which emphasizes the manipulation of sparse matrices
- A very user-friendly interface based upon EASE+

Expert-EASE Systems is a product-oriented company with a proven track record in the U.S. and international marketplaces. Our goal is to use the Phase II project to develop a commercial multi-microprocessor which can be used in a back-end configuration with general purpose computer, such as a MicroVAX.

In summary, based upon our successful Phase I project and our proven track record in developing commercial products we are firmly convinced that we can deliver an initial, 15 Transputer system to NASA/Langley within 19 months after the start of the Phase II effort. This will be shortly followed by the marketing of the product to private businesses and government agencies as a low-cost, high performance answer to their demands for additional computing power.

SUMMARY (Cont'd)

3. Large, Demand-Driven Markets

   - Focus on Computational Structural Mechanics

   - Incorporate Other Functions of Interest to NASA
     - Stability
     - Control
     - Optimization

   - Generalize to Other Markets
     - Signal Processing
     - Medical Imaging